SINGLE-EVENT UPSET IN ADVANCED POWERPC MICROPROCESSORS*

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***Abstract* – Proton and heavy-ion single-event upset susceptibility has been measured for the Motorola PowerPC7400. This device has much smaller feature size and lower core voltage compared to the PowerPC750. The results show that the more advanced device has about the same low upset susceptibility, despite the scaling and design advances, suggesting that COTS-based processors can be used in selected space applications.**

I. INTRODUCTION

In recent years there has been increased interest in the possible use of unhardened commercial microprocessors in space because of the increased performance compared to hardened processors. However, unhardened devices are susceptible to upset and degradation from radiation, and more information is needed on how they respond to radiation before they can be used in space. Only a limited number of advanced microprocessors have been subjected to radiation tests, and the majority have been older device types which are designed with much larger feature sizes and higher operating voltages than modern devices [1-7].

Single-event tests were performed to provide estimates of upset rates for various space applications, including earth orbiting, deep space, and planetary exploration missions. These results help to determine what kinds of effects are produced in advanced microprocessors by space radiation and how they can be detected and overcome. Complex failure modes are of particular interest because they potentially limit ways in which errors and malfunctions can be detected and corrected by hardware or software techniques.

The PowerPC750 was co-designed by IBM and Motorola. The first generation PowerPC750 can operate at speeds of up to 350 MHz. We have previously reported single-event measurements on Motorola and IBM PowerPC750 processors [1]. The PowerPC74xx series incorporates a more advanced processing unit (AltiVec). The AltiVec unit can perform four single precision floating point or sixteen byte calculations, in a single cycle. Table 1 shows how the PowerPC7400 fits with previous and recent generations of the PowerPC family. Note that the feature size of the PowerPC7400 is reduced from 0.29 to 0.20 μm compared to the PowerPC750, with the core voltage reduced from 2.5 to 1.8 V. The larger die size of the PowerPC7400 is due to the more advanced design. Recently announced, PowerPC7445/7455 are the latest generation of the Motorola PowerPC family which are fabricated with Silicon-On-Insulator, SOI, technology.

Table 1. Summary of Motorola's PowerPC Family of Advanced Processors.

Device	Feature Size (μm)	Die Size (mm^2)	Core Voltage (V)	Maximum Operating Frequency (MHz)
MPC603 (G2)	0.50	196	2.5	300
MPC750 (G3)	0.29	67	2.5	350
MPC7400 (G4)	0.20	83	1.8	500
MPC7450 (G4)	0.18	106	1.6	867
MPC7445 (G4)	0.18	TBD	1.3	800
MPC7455 (G4)	0.18	TBD	1.6	1000

This paper reports test results for the PowerPC7400. The test examined upsets in the AltiVec registers, the L1 data cache and their tags, L2 tags, and the Translation Lookaside Buffer (TLB of the Memory Management Unit, MMU), as well as overall results for processor functionality. Tests were done using energetic protons and heavy-ion beams. The protons have sufficient range to penetrate the packaging material of the PowerPC7400, but heavy-ion beams that were available have limited range and cannot penetrate the package. In order to overcome this limitation, tests were done on specially prepared units that were thinned so that irradiation from the back of the die penetrated to the front side of the die.

II. EXPERIMENTAL METHOD

Radiation testing was done using a development board from Motorola known as "Yellowknife". This board was chosen because it eliminated the large engineering effort that would

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be required to design a custom test board for the processor and also provided a very basic PROM-based system monitor instead of a complex operating system. This provides far better diagnostic information and control of processor information during SEE testing compared to more advanced operating systems. The Yellowknife board has a small daughter card for the processor and cache with no active components underneath, which is important for proton beam penetration. This allowed us to shield other components on the board during proton tests, assuring that the measured response was entirely due to effects within the processor. The only external communication channels provided on the Yellowknife are a simple serial connection for a "dump" terminal and a JTAG port. An Agilent Technology 5900B JTAG probe was used for our tests. This probe made it possible to interrogate the processor even after unexpected events occurred (such as operational errors during irradiation).

The methodologies used in these tests are briefly described below. Detailed descriptions of them can be found in Refs. 1 and 8.

A number of assembly language software programs were written to enable errors in various sections of the processor to be determined. It was possible to design software that primarily exercised specific registers or regions, and thus allowed the number of errors to be determined for various registers. During some of the tests, the processor became non-functional (program "hangs"). In most cases it was not possible to determine the underlying cause of those malfunctions (particles from the accelerator strike random locations within the processor), but the relative occurrence of such malfunctions was measured and can be compared to the upset rate obtained for internal registers or other functions of the processor. Minimizing processor activity during irradiation essentially reduces the number of internal operations, thereby making the operation susceptible to errors in only a few internal locations. In our test method, "do nothing with strip chart", the processor was programmed to perform a one word instruction in a small infinite loop and write a register snapshot to a strip chart in the physical memory every half second. After the irradiation ended, an external interrupt triggers a program to count state changes in internal registers or the data cache.

A more complex method was required to examine errors in the L1 data cache. Because of limitations in the firmware of PowerPC7400, we were not able to access the instruction cache and measure its error upsets. Upsets in the data cache were counted with a special post beam software. The data cache was initialized under specified conditions prior to irradiation and then disabled. Then a clearly recognizable pattern, designed to be distinctly different from contents of the cache, was placed in the external memory space covered by the cache. Comparing the cache contents after irradiation provided verification of the cache contents. Tag upsets, as well as upsets of the data valid flag, were detected by monitoring the distinctly different pattern. The tag and data valid upsets were thus distinguished and counted separately from upsets of the data bits themselves.

There is no instruction that directly accesses the contents of the TLB. Therefore, we applied the following methodology to measure upsets in the TLB. Prior to irradiation, the memory was divided into two separate data groups. Each data group was filled with its own physical address. The two Page Table Entry Groups were set in two different locations of memory. The first Page Table Entry Group mapped to the first section of the filled area. The second Page Table Entry Group mapped to the second data group of memory. Then the Memory Management Unit was enabled, and memory was mapped using the first Page Table Entry Group. This method caused TLB's to be filled by the first Page Entry Group. The Memory Management Unit was disabled and an infinite loop was executed during the irradiation. After the irradiation had ended, an external interrupt exited the loop and enabled the Memory Management Unit with pointers to the second Page Table Entry Group. The Memory Management Unit checked the TLB's to obtain a valid Page Table Entry. In case there was an upset and no valid entry, the Memory Management Unit commenced to obtain a valid Page Table Entry from the second Page Table Entry Group. Data was read from the first group and compared with their addresses. Differences indicate at least one upset bit the corresponding Page Table Entry in the cached TLB.

Proton tests with energies above 65 MeV were performed at the Indiana University Cyclotron Facility. Tests at lower energies were done at the UC Davis cyclotron. Because of sufficient range of protons to penetrate the packaging material of the PowerPC7400, tests were done in air without any need for package modification.

Heavy-ion tests were performed at the Texas A&M accelerator. This facility produces the long-range ions needed for SEU testing through thick materials. Particularly, the 25 and 40 MeV/amu beams are quite penetrating, and it is practical to do irradiations in the air rather than in a vacuum. However, the total thickness of the die for PowerPC7400 is ~719 μm and, in contrast to proton beams, the limited range of heavy-ion beams does not allow them to penetrate the package. The "flip-chip" design of the PowerPC7400 does not allow the device to be "delidded" without destroying the pad and bonding connections. In order to get around the delidding problem, we grounded down the back surface of the PowerPC7400. This reduced the total thickness of the die to 50-200 μm without impacting the electrical characteristics. The thin die did not affect charge collection because it has a thin-epitaxial layer. There is good agreement for SEU results obtained from different thicknesses of the PowerPC processor, after correcting for energy loss through the thinned substrate [8].

A custom heat sink with a hole for the processor die was used to conduct heat away from the package, and a thermocouple was used to measure temperature increases during the time that the device operated. Also, a routine was developed to read out the processor's junction temperature. In heavy ion measurements a circulating water circuit was used to cool the Yellowknife boarding frame, heat sink and JTAG probe.

III. TEST RESULTS

A. Proton Tests

The methods discussed in the previous section were used to measure the single-event upset rates for Registers, Data-Cache Memory, Data-Cache Tags and Flags, and TLB. These measurements were done for various proton energies. The measurement for Registers includes General Purpose Registers, GPR, Floating Point Registers, FPR, Special Registers, SPR, and AltiVec Registers.

Figure 1 shows results of cross section measurements for the PowerPC7400 Data-Cache Memory bits for "1" to "0" and "0" to "1" transitions. The cross section for transitions between "1" and "0" are statistically identical. The threshold cross section is about 5-7 MeV, and the saturated cross section is about $3x10^{-14}$ cm^2/bit, which is in agreement with data for the PowerPC750 with its feature size of 0.29 μm[1]. This indicates that the higher density and increased speed of the PowerPC7400 does not increase the sensitivity of the registers to upset from protons. The low threshold behavior is reasonable if one considers that the cache memory must fit within a restricted area within the processor. The lower saturation cross section is probably due to reduced device area in the high-speed cache registers. The large number of storage locations within the data cache allows more statistically significant numbers of errors to be measured, decreasing the error bars due to counting statistics. The cross section for D-Cache Tags and Flags shows similar behavior, except the saturation cross section is about $1x10^{-9}$ cm^2/bit.

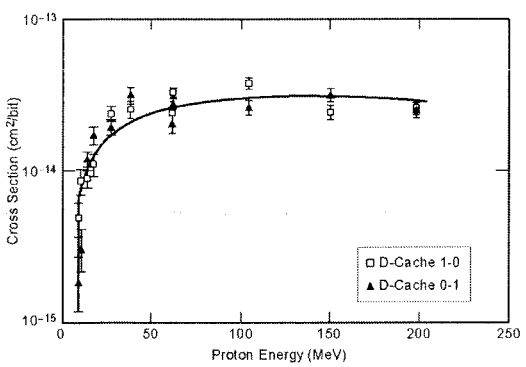

Figure 1. Cross-section vs. proton energy for transitions between "1 to 0" and '0 to 1" for the data cache bits in the PowerPC7400 processor. The error bars are ~2 sigma and result from Poisson statistics. The curve is a guide for the eye.

Figure 2 shows results of cross section per bit measurements for TLB of the PowerPC7400 MMU versus proton energy. For comparison we show our previous measurements for the PowerPC750 [1]. The saturated cross section is about $5x10^{-14}$ cm^2/bit and the threshold energy is about 15 MeV, which are in agreement with results for the PowerPC750.

B. Heavy-Ion Tests

We measured the single-event upset rates for the AltiVec Registers, Data-Cache Memory, Data-Cache Tags and Flags, and the TLB. These measurements were done for LET ranges between 3.8 and 60 MeV-cm^2/mg.

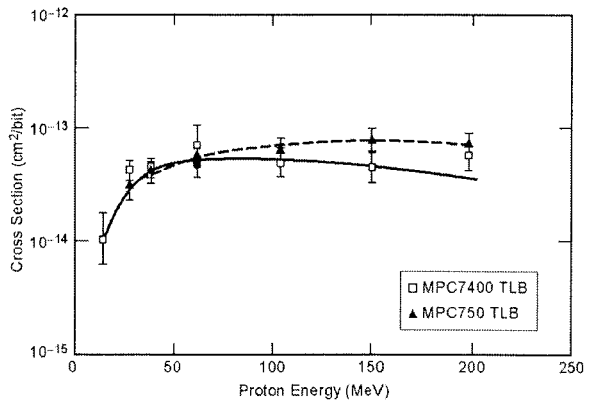

Figure 2. Proton single-event–upset cross-section for TLB's of the PowerPC7400 and PowerPC750. The solid and dashed curves are a guide for the eye.

Figure 3 displays results of cross section measurements for the PowerPC7400 Floating Point Register for "1" to "0" transitions. The LET threshold is about 5 MeV-cm^2/mg, and the saturated cross section is about $1x10^{-7}$ cm^2/bit. The cross section for "1" to "0" transitions is the same as for "0" to "1" transitions. These data were taken with several parts with different thicknesses. The LET at the device surface had to be corrected to allow for decrease in beam energy as ions traversed the device from back to the sensitive top surface of the device. There is a good agreement for results obtained from different thicknesses. This is expected since advanced processors require a fairly thin epitaxial layer and there is no major charge collection differences between devices with different thicknesses. It is interesting to compare these results with earlier results for the PowerPC750. The LET threshold and saturated cross section for the two types of processor are the same. Thus, the increased die size, decreased feature size and decreased internal core voltage of the PowerPC7400 did not appear to have changed the sensitivity to the single-event upset very much.

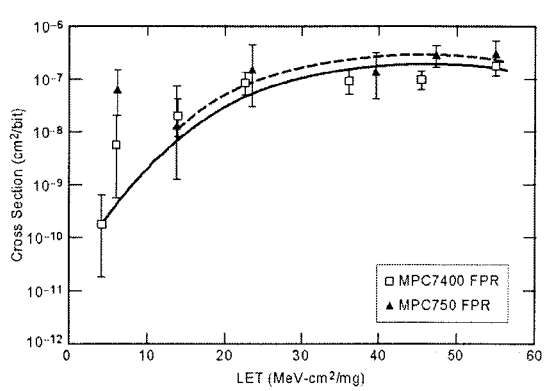

Figure 3. Heavy-ion single-event upset cross section for floating-point registers in the PowerPC7400 and PowerPC750 for "1" to "0" transitions. The solid and dashed curves are a guide for the eye.

Figure 4 shows results of heavy-ion measurements for the TLB of the PowerPC7400 MMU. The saturated cross section is about $4x10^{-8}$ cm^2/bit. For comparison, the figure shows data for the PowerPC750. The saturated cross section is

slightly lower than the PowerPC750. This might be related to smaller die size for MMU unit in the PowerPC7400. We plan to do the measurements at lower LET to compare the threshold cross section with the result for the PowerPC750. The final paper will include these results.

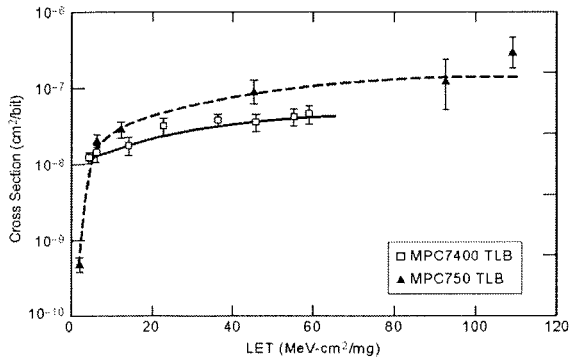

Figure 4. Comparison of the heavy-ion single-event-upset cross-section for the TLBs of the PowerPC7400 to those of the PowerPC750. The solid and dashed curves are a guide for the eye.

We also examined program "hangs". The PowerPC7400 hangs with both protons and heavy ions. We refer to hangs as a failure to respond to an external interrupt after the irradiation was ended. There appears to be many types of hangs. We have not been able to thoroughly identify them. In order to roughly scope problems with hangs, we calculated the hang cross section defined as the number of times the processor would not respond to the external interrupts divided by the total fluence to which the processor had been exposed. This was done for each LET. Figure 5 shows results of hangs in heavy-ion measurements. The threshold LET appears comparable to that obtained for register errors, but cross section is lower. The cross section per device due to "hangs" is about 10^{-5} cm^2 for LETs above 5 MeV-cm^2/mg that agrees with the PowerPC750 results. From an application standpoint, program "hangs" can be severe problems even if they occur infrequently because of the difficulty of identifying the malfunction and determining how to restore operation afterwards. Although we were able to reduce the impact of program "hangs" for test software that was tailored for single-event testing, program "hangs" are expected to be a major issue for most application software written in higher level languages. Thus, additional work needs to be done in order to categorize these malfunctions as well as to determine whether a method can be developed to detect them when more complex software is used.

IV. CONCLUSIONS

There are standard techniques that have been developed over many years to calculate single-event upset rates directly from experimental results presented here [9,10]. The advanced commercial PowerPC microprocessors are slightly less sensitive to single-event upset compare to earlier generations of the PowerPC microprocessors. Although the PowerPC7400 has smaller, sub-micron geometry, lower

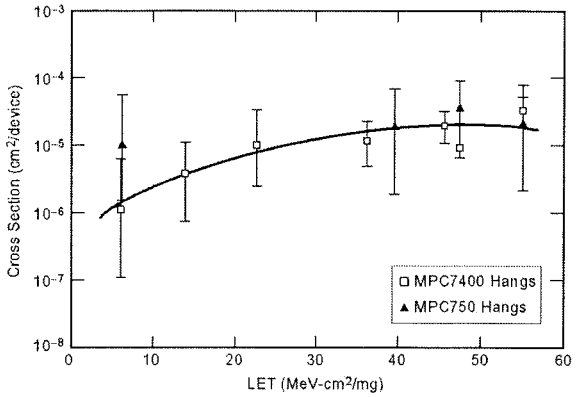

Figure 5. Heavy-ion cross sections for the PowerPC750 and the PowerPC7400 hangs. The curve is a guide for the eye.

internal core voltage and design advances, its proton and heavy ion upset susceptibility is only slightly lower than the PowerPC750. The low space rates, immunity to latchup, and relatively low power consumption, allow them to be used successfully in many space environments. They can be used in data analysis or instrument control applications where occasional malfunctions or errors from single-event upset can be tolerated and corrected.

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