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Embedded Passives Emulator FY2008 Interim Report

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Summary

The National Aeronautics and Space Administration Electronic Parts and Packaging (NEPP) Program has been evaluating state-of-the-art Embedded Passive Technology for the printed circuit board (PCB) industry for the past several years and has conducted its own testing on embedded passive coupons (resistors and capacitors) [1-3]. This document is a progress report of the work performed through fiscal year 2008 by NASA and the Navy to convert an existing printed wiring board (PWB) design to a design that incorporates embedded passive components. The work is being performed through a memorandum of understanding (MOU) between the NEPP Program (NASA) and the Naval Surface Warfare Center (NSWC) Crane Emerging Critical Interconnect Technology (ECIT) Program.

NSWC Crane's ECIT Program has funding to convert two PCB designs from the military and aerospace industry to a PCB design with embedded passives. ECIT will provide a design team that will take a well characterized design and convert it to an embedded design. They will also provide electrical modeling and layout expertise as well as build the PWB in their facility in Indiana. NEPP, through the Jet Propulsion Laboratory (JPL), will assemble any passives deemed not suitable for embedding and the active components and electrically test the new design to the existing (non-embedded) design. Reliability testing of the embedded PCB assembly is planned as well as joint papers, reports, and Institute-for-Printed-Circuits (IPC) interactions.

1 Introduction: NSWC Crane and NEPP Team-Up

Eventually, designs will start out as embedded, but today's designs start out in a more conventional manner where all of the parts are decided before the design is started. For a design to achieve maximum benefit, the reduction of contributions to vias, traces, and discrete components must be taken into account. When dealing with embedded passives, a one-for-one tolerance does not necessarily apply between discrete and embedded passives. Converting an existing design to an embedded-passives design is not a trivial task and a team approach is required to maximize the benefit.

Since the dramatic decline of the US captive printed circuit board fabrication and R&D, and the formation and demise of the Interconnection Technology Research Institute (ITRI), Ron Thompson (formerly a branch manager at NSWC Crane) and David Bergman (Vice President of the IPC) formed and successfully found funding for the ECIT at NSWC Crane. Their goal for ECIT is to aid the North American PCB manufacturing industry by researching state-of-the-art advances in design, development, and manufacturing processes. NSWC Crane has a complete state-of-the-art PCB manufacturing facility, comprehensive failure analysis lab, environmental test and evaluation lab, and extensive computer modeling capabilities to support this goal.

In 2005, at IPC Works, the ECIT team created an opportunity for the Original Equipment Manufacturers (OEMs) to participate in an emulator project. Basically, OEMs with a heritage design having characteristics attractive for embedding passive components could submit this design to ECIT as an emulator candidate. If selected, the ECIT staff would work with the OEM in choosing the best components to embed and the best material(s) to use. ECIT would redesign

the board(s) within the constraints established by the OEM, manufacture the bare boards, perform reliability studies on the embedded components, and deliver the bare boards to the OEM. The OEM, in turn, would assemble and test the boards, comparing the results to the heritage design.

The cost of the redesign, bare board manufacture, and testing is borne by ECIT. The cost of assembly and test is borne by the OEM. The design tools being used are Mentor Graphics Expedition's integrated parametric embedded passives module. Modeling and analysis tools are also being used to evaluate the resulting design. OEM participation requires their willingness to share the performance results with industry. Intellectual Property (IP) associated with the design will be protected by ECIT.

Ideally, there should be a design team consisting of a designer, project engineer/manager, board manufacturer, and material suppliers. All members must be included in the selection and design process. Every aspect of the design must be thoroughly thought through or the process can be a painful one. It is a process where all of the boxes must be checked. Embedded passives are generally new materials and these materials affect the design. The PCB fabricator must gain experience and develop robust processes as parts have to be placed where they are normally not placed. Libraries or parameters need to be created. Thus, it is a learning process for everyone. An experienced partner, such as NSWC Crane, can provide valuable tools in converting a design from a conventional to an embedded one.

The ECIT team selected two designs from the Military and Aerospace industry, one from Harris Corporation, and one from JPL/NASA. The design submitted to the ECIT team from NASA/JPL was for an assembly capable of operating within the temperature range from -120°C to $+80^{\circ}\text{C}$.

This particular assembly can be tailored to actuate virtually any motor while the electronics are high density and low mass. For those reasons, it was thought that this design would make a good candidate for the embedded-passives emulator project. The assembly employs more than 1170 components, a large number which negatively impacts its reliability, power consumption, mass, and manufacturability, and results in a high manufacturing cost. If this task is successful in eliminating a large number of passives components, it is believed that the manufacturing cost, mass, and power consumption would all be reduced, thereby, making it more suitable for flight systems.

2 PWB Design

The key features of the assembly are its survivability, small volume and mass, and serial interface. It can survive and operate in extreme hot and cold environments; is radiation hardened; and is packaged to survive high dynamic stress of launch, landing, and pyrotechnic events. The design consists of eight PWBs connected by using rigid-flex PCB technology. The PCBs are folded into the shape of a cube, yielding its final form. A photograph of the design is shown in Figure 1.

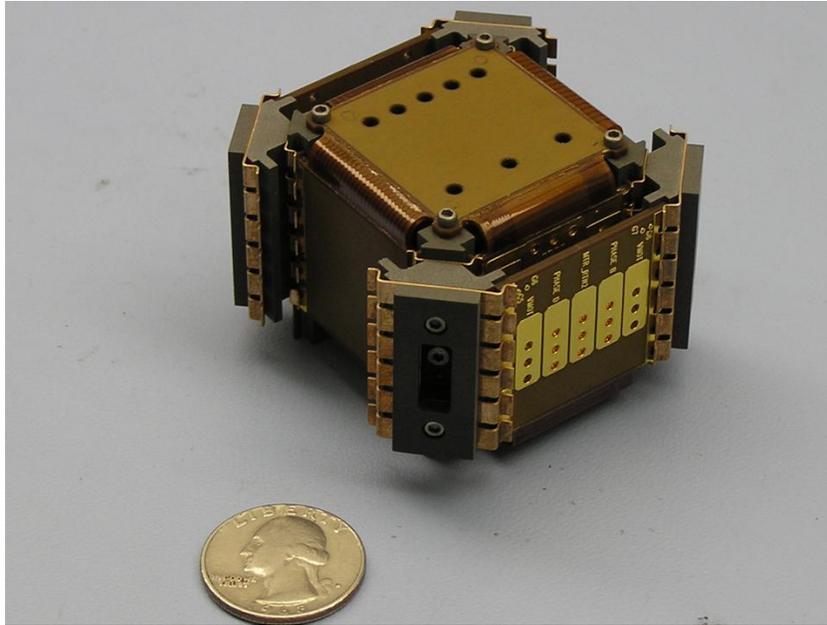


Figure 1: A prototype photograph of the assembly (actual size)

Each small PWB, referred to as a “petal,” contains a specific function such as motor amplifier, power, communication, motor encoder/resolver, analog and digital signals, etc. The assembly technology utilized in the design is chip-on-board (COB) with surface mount technology for capacitors and some resistors. Due to the proprietary nature of the design, details cannot be described in this document. Also, due to the complexity of this design, it was decided by the JPL and NSWC Crane team that the digital portion of the cube would be an appropriate undertaking for the project. In the original design, the digital “petals” were characterized separately from the final assembly and, therefore, could be compared to an embedded-passives version. The PCB is approximately 60 mils thick comprised of 12 layers, including several analog and digital power and ground planes of varying thicknesses. The prepreg material is polyimide-coated fiberglass.

An unfolded cube assembly is shown in Figure 2 with the digital “petals” circled in red.

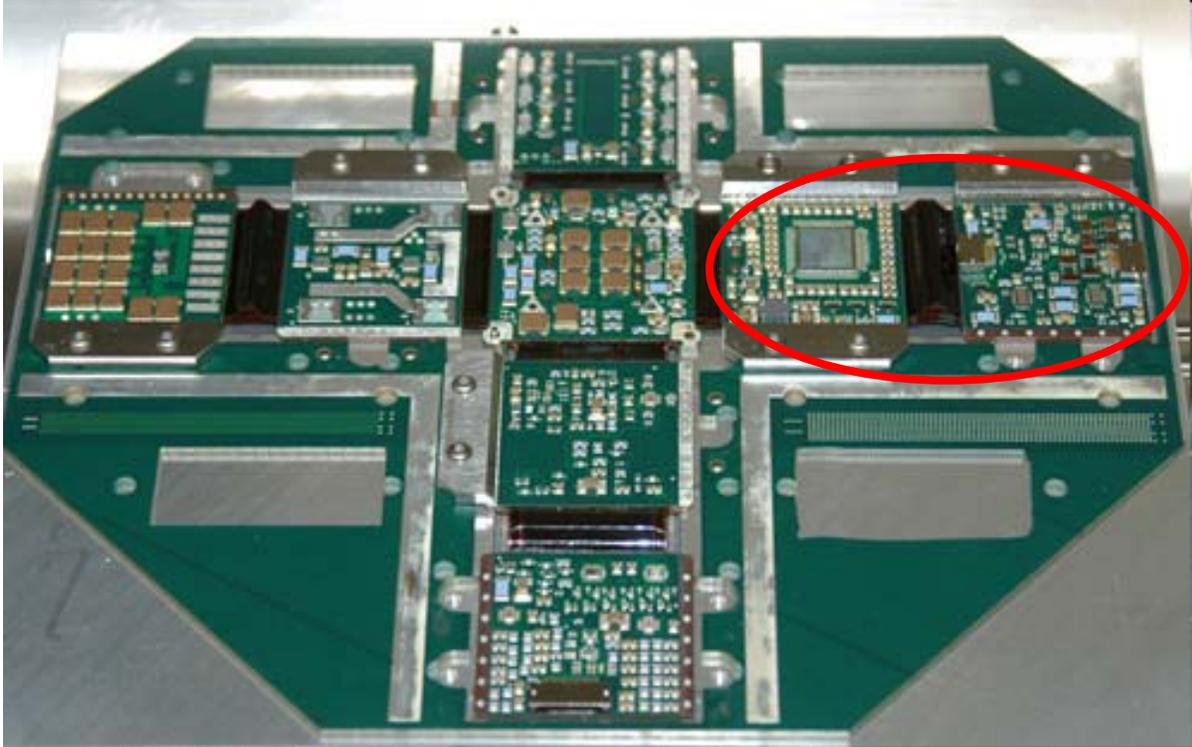


Figure 2: Unfolded PWB version of the assembly showing the rigid-flex connection between each PWB. The section of the design that is being converted to (primarily) embedded passives is circled in red.

3 Components Selected for Embedding

Following the transfer of files containing the design and bill of materials to the team members at NSWC Crane, the capacitors and resistors were categorized by the JPL team. The team used three categories: 1) candidates for embedding, 2) components not recommended for embedding, and 3) parts with tolerance tracking requirements (may or may not be possible for embedding). Table 1 illustrates the number of components and the recommendations for passive components that can be embedded from the JPL design team.

Table 1: Passive components candidates for embedding

Item	Quantity	Reference	Part	Part Number	PCB Footprint	Tolerance	Power	Temp Char
1	102	C25,C26,C27,C28,C29,C30, C32,C33,C34,C35,C36,C37, C38,C39,C40,C41,C42,C43, C44,C45,C46,C47,C48,C49, C50,C51,C52,C53,C54,C55, C56,C57,C58,C59,C60,C61, C62,C63,C64,C65,C66,C67, C68,C69,C70,C71,C72,C73, C74,C75,C79,C81,C83,C85, C87,C88,C89,C90,C92,C93, C94,C96,C97,C104,C106, C108,C110,C112,C113,C114, C115,C117,C118,C119,C121, C122,C167,C168,C169,C172, C177,C182,C188,C189,C190, C195,C196,C197,C201,C203, C204,C209,C215,C216,C218, C219,C220,C234,C361,C363, C387,C403	0.1U	C0805C104J4RAG	c0805	5%		X7R
2	10	C31,C76,C165,C166,C180, C184,C207,C211,C362,C364	1U	1206YC105JA72A	c1206	10%		X7R
3	10	C77,C82,C102,C107,C175, C178,C187,C199,C206,C214	100P	C0603C101F4GAG	c0603	1%		COG
4	15	C78,C84,C91,C95,C101, C103,C109,C116,C120,C126, C183,C194,C202,C210,C217	10U	1812YC106JA72A	c1812	10%		X7R
5	10	C80,C86,C105,C111,C176, C181,C185,C200,C208,C212	1000P	C0805C102F4GAG	c0805	1%		COG
6	2	C98,C123	0.039U	C0603C393F4RAG	c0603	1%		X7R
7	2	C99,C124	0.0039U	C0805C392F4GAG	c0805	1%		COG
8	2	C100,C125	510P	C0805C511F4GAG	c0805	1%		COG
9	8	C170,C171,C173,C174,C179, C186,C205,C213	51P	C0603C510F4GAG	c0603	1%		COG
21	4	RN2,RN3,RN4,RN5	10K	WCLB-017-10001F	die_wclb	1%	0.05W/R	50ppm
22	6	R32,R37,R71,R108,R473, R483	10	P2010E10R0CG	r2010	0.25%	1W	25ppm
23	15	R38,R44,R59,R61,R62,R68, R70,R80,R96,R98,R99,R105, R107,R474,R484	10K	P0402E1002DG	r0402	0.50%	0.05W	25ppm
24	26	R39,R42,R49,R52,R53,R57, R60,R63,R66,R67,R69,R79, R86,R89,R90,R94,R97,R100, R103,R104,R106,R165,R166, R235,R476,R486	10	P0402E10R0DG	r0402	0.50%	0.05W	25ppm

Table 1, cont'd: Passive components candidates for embedding

Item	Quantity	Reference	Part	Part Number	PCB Footprint	Tolerance	Power	Temp Char
25	15	R40,R45,R58,R82,R95,R163, R164,R211,R233,R251,R475, R477,R478,R479,R485	5.1K	P0402E5101DG	r0402	0.50%	0.05W	25ppm
26	15	R41,R48,R56,R65,R78,R83, R93,R102,R177,R187,R212, R227,R260,R278,R511	10	P0805E10R0DG	r0805	0.50%	0.2W	25ppm
27	7	R43,R81,R215,R230,R263, R281,R513	1K	P0805E1001DG	r0805	0.50%	0.2W	25ppm
28	4	R46,R47,R84,R85	100K	P0402E1003DG	r0402	0.50%	0.05W	25ppm
29	4	R50,R54,R87,R91	40.2K	P0402Y4022LG	r0402	0.01%	0.05W	10ppm
30	5	R51,R55,R88,R92,R236	300K	P0805Y3003LG	r0805	0.01%	0.2W	10ppm
31	2	R64,R101	47K	P0402Y4702LG	r0402	0.01%	0.05W	10ppm
32	2	R72,R109	499	P0805E4990DG	r0805	0.50%	0.2W	25ppm
33	2	R73,R110	4.99K	P1005Y4991LG	r1005	0.01%	0.25W	10ppm
34	2	R74,R111	90.9K	P0402E9092DG	r0402	0.50%	0.05W	25ppm
35	2	R75,R112	806K	P0402H8063DG	r0402	0.50%	0.05W	50ppm
36	6	R76,R113,R167,R168,R171, R173	51	P2010K51R0JG	r2010	5%	1W	100ppm
37	10	R77,R114,R201,R202,R203, R206,R240,R241,R243,R246	160	P0402Y1600PG	r0402	0.02%	0.05W	10ppm
38	6	R169,R170,R172,R174,R175, R176	51K	P0402E5102DG	r0402	0.50%	0.05W	25ppm
39	6	R178,R188,R213,R228,R261, R279	1K	P0505Y1001LG	r0505	0.01%	0.125W	10ppm
40	4	R179,R180,R189,R190	32K	P0402Y3202LG	r0402	0.01%	0.05W	10ppm
41	8	R181,R182,R183,R184,R191, R192,R193,R194	40.0K	V15X10T40K000T	v15x10	0.01%	0.15W	2.2ppm
42	5	R185,R186,R195,R196,R222	10K	P0402Y1002LG	r0402	0.01%	0.05W	10ppm
43	17	R197,R199,R204,R205,R207, R208,R210,R221,R225,R234, R238,R244,R245,R247,R248, R250,R252	5.1K	P0402Y5101LG	r0402	0.01%	0.05W	10ppm
44	2	R198,R237	100	P0805E1000DG	r0805	0.50%	0.2W	25ppm
45	4	R200,R209,R242,R249	499K	P1005Y4993LG	r1005	0.01%	0.25W	10ppm
46	5	R214,R229,R231,R262,R280	80.6K	P0402E8062DG	r0402	0.50%	0.05W	25ppm
47	1	R223	1.24K	P0805Y1241LG	r0805	0.01%	0.2W	10ppm
48	1	R224	2.49K	P0805Y2491LG	r0805	0.01%	0.2W	10ppm
49	1	R226	15K	P0402Y1502LG	r0402	0.01%	0.05W	10ppm
50	1	R253	20K	P1005Y2002LG	r1005	0.01%	0.25W	10ppm
51	1	R254	1.8K	P0402Y1801LG	r0402	0.01%	0.05W	10ppm
52	1	R255	2.7K	P0402Y2701LG	r0402	0.01%	0.05W	10ppm
53	1	R256	4.02K	P0402Y4021LG	r0402	0.01%	0.05W	10ppm
54	1	R257	6.04K	P0402Y6041LG	r0402	0.01%	0.05W	10ppm
55	1	R258	8.98K	P0402Y8981LG	r0402	0.01%	0.05W	10ppm
56	1	R259	13.7K	P0402Y1372LG	r0402	0.01%	0.05W	10ppm
57	3	R480,R481,R482	2K	P0805E2001DG	r0805	0.50%	0.2W	25ppm
58	1	R526	1M	P0805H1004DG	r0805	0.50%	0.2W	50ppm

Table 2 contains a subset of the list of components from Table 1. These components are the passive devices that have tracking requirements for performance reasons. Many of these components are specified to the highest precision level because they are part of a circuit that must have two or more tracks over temperature.

Table 2: Passives that require high tolerance or tracking (subset of Table 1)

Item	Passive Type	Reference	Part	Temp Char
MATCHED	CAP	C105/C111	1000p	COG
MATCHED	CAP	C110/C112	0.1u	X7R
TOLERANCE	CAP	C177	0.1u	X7R
MATCHED	CAP	C180/C184	1u	X7R
MATCHED	CAP	C181/C185	1000p	COG
TOLERANCE	CAP	C204	0.1u	X7R
MATCHED	CAP	C207/C211	1u	X7R
MATCHED	CAP	C208/C212	1000p	COG
MATCHED	CAP	C77/C88	100p	COG
MATCHED	CAP	C80/C86	1000p	COG
MATCHED	CAP	C85/C87	0.1u	X7R
TOLERANCE	RESISTOR	R101	47K	0.01%
TOLERANCED	RESISTOR	R181-R184	40.0K	0.01%
TOLERANCED	RESISTOR	R191-R194	40.0K	0.01%
MATCHED	RESISTOR	R50/R54	40.2K	0.01%
MATCHED	RESISTOR	R51/R55	300K	0.01%
TOLERANCE	RESISTOR	R64	47K	0.01%
MATCHED	RESISTOR	R87/R91	40.2K	0.01%
MATCHED	RESISTOR	R88/R92	300K	0.01%
MATCHED	RESISTOR	R201/R202	160ohm	0.02%
MATCHED	RESISTOR	R203/R206	160ohm	0.02%
MATCHED	RESISTOR	R240/R241	160ohm	0.02%
MATCHED	RESISTOR	R243/R246	160ohm	0.02%
MATCHED	RESISTOR	R179/R180	32K	0.05%
MATCHED	RESISTOR	R185/R186	10K	0.05%
MATCHED	RESISTOR	R189/R190	32K	0.05%
MATCHED	RESISTOR	R195/R196	10K	0.05%
MATCHED	RESISTOR	R200/R209	499K	0.05%
MATCHED	RESISTOR	R204/R207	5.1K	0.05%
MATCHED	RESISTOR	R205/R206	5.1K	0.05%
MATCHED	RESISTOR	R242/R249	499K	0.05%
MATCHED	RESISTOR	R244/R247	5.1K	0.05%
MATCHED	RESISTOR	R245/R248	5.1K	0.05%
MATCHED	RESISTOR	R46/R47	100K	0.05%
MATCHED	RESISTOR	R84/R85	100K	0.05%

One of the primary concerns for embedding resistors in a PC board design is the fact that the tolerance is much less than discrete resistors unless the resistors are placed on the surface and laser trimmed. Trimmed resistors can present their own set of problems as they are generally placed on the outer surfaces of the board to allow for a laser trimming process, which produces a more precise resistor but usually leaves the bare resistor material exposed. In this design, NSWC Crane will have the precision resistors laser trimmed on inner layers. Even though laser trimming the resistors will never yield precision resistors as precise as the discrete resistors specified in this design, embedded resistors have some properties that may make up for this shortcoming. Embedded resistor materials lead to the following benefits:

1. Improved line impedance matching
2. Shorter signal paths and reduced series inductance
3. Elimination of the inductive reactance of the Surface Mount (SMT) device
4. Reduced cross talk, noise, and Electromagnetic Interference (EMI)

For high speed designs and short rise times, embedded resistor tolerances are not nearly as important as the elimination of the inductive reactance of the SMT chip components, vias, and traces [4]. In actuality, the resistor tolerance is a combination of the initial mismatch of the device value and line impedance, the device tolerance (percentage), and the series inductance and inductive reactance of the device. For these applications, a 10% embedded resistor is better than a 1% SMT resistor when series inductance and inductive reactance of the entire interconnect discrete resistance (SMT chip, via, and trace) and resistor are taken into account [4]. Also, where tracking is required, as in this design, the resistor material is planar in nature with resistors etched and singulated to form individual resistors. Since each resistor is made from the same planar material, they will track uniformly.

Similar concerns regarding embedded capacitors exist. The embedded material's dielectric properties do not generally allow for a one-to-one replacement (embedded versus discrete). Various manufacturers' embedded capacitor laminate materials have been successfully implemented on a number of OEM designs to replace large quantities of discrete decoupling capacitors from the board surface. Some of the data from these board designs are shown in Table 3 [5].

It can be seen that in every case, the use of the distributed embedded capacitance allowed the elimination of at least 60% of the discrete capacitors. In most cases, it was at least 75% and in two cases, all of the discrete decoupling capacitors were removed. In one case, more than 500 capacitors were eliminated from the board design. It is also very important to note that only a very small amount of embedded capacitance was needed to replace a very large amount of discrete capacitance (each nF of embedded capacitance replaced 10 to 40 nF of discrete capacitance).

Once the discrete passives in the circuit were identified by the JPL design team, the team from NSWC Crane implemented their decision tree to assess whether the design could benefit from the embedding process. Figure 3 shows the flowchart used to decide whether to embed the JPL/NASA design. Obviously, the decision to go forward was made.

Table 3: Examples of decoupling capacitors replaced by embedding capacitance [5]

Design	Discrete Capacitance Removed (nF)	Embedded Capacitance (nF)	Ratio of Removed to Embedded	% of Total Discrete Capacitance Removed
EDC TV1	330 <i>33 x 0.01 uF</i>	105	3.1	100%
OEM A	12,600 <i>126 x 0.1 uF</i>	300	42.0	>75%
OEM B	6,310 <i>62 x 0.1 uF</i> <i>11 x 0.01 uF</i>	210	30.0	>60%
OEM C	3,180 <i>29 x 0.1 uF</i> <i>28 x 0.01 uF</i>	305	10.4	>75%
OEM D	52,900 <i>529 x 0.1 uF</i>	1970	26.9	>75%
OEM E TV	9,900 <i>99 x 0.1 uF</i>	660	15.0	100%

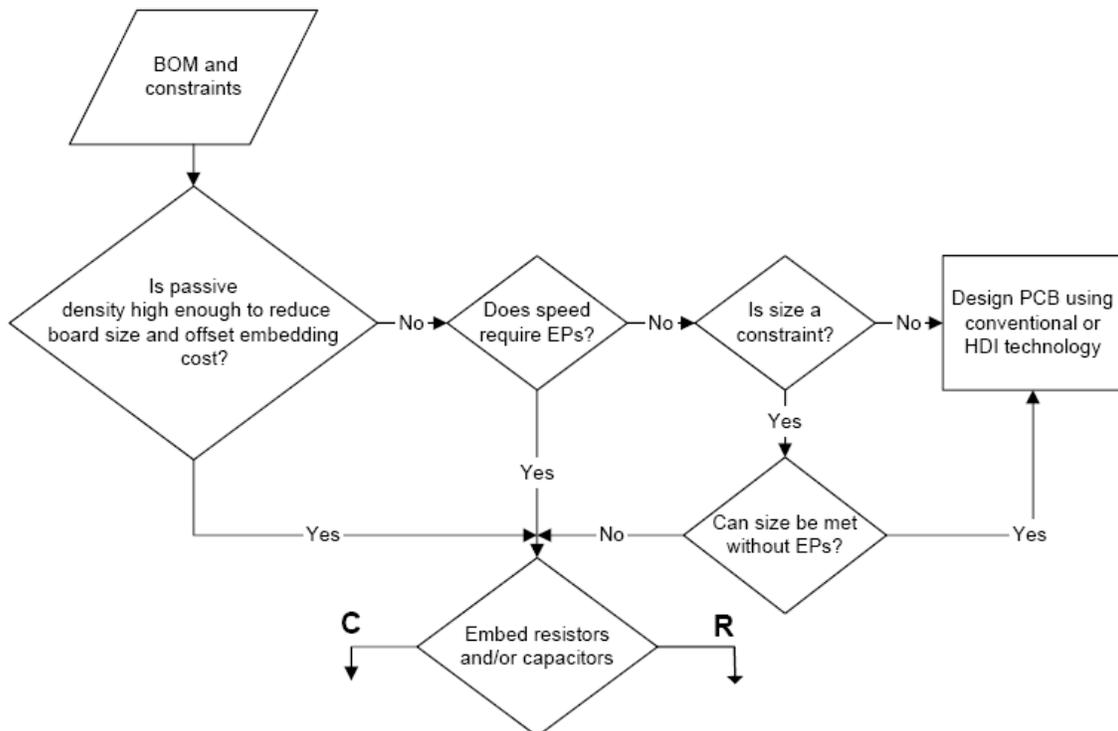


Figure 3: The decision tree shown as a flow diagram used to decide whether to embed components.

Once it was decided to move forward with the design, the next steps were to implement the design with inputs from the design team and to assess which passives could be embedded by using the flowchart in Figure 4. The NSW Crane team had completed the first emulator project and was able to apply the lessons learned from that project to this project. With NSW Crane's guidance and JPL's design inputs, passive component materials sets were selected with a fairly large number of passives eliminated. A summary of the resistors and capacitors is listed below:

- 2 resistor layers; 1 with 1000 ohm/square and 25 ohm/square materials
 - 93 resistors could be embedded using the 1000 ohm/square metal
 - 65 resistors could be embedded using the 25 ohm/square metal
 - 40 resistors could not be embedded based on the large value required (32K and higher)
- Capacitor materials will be C-Ply (3M material) for embedding the decoupling capacitors (0.1 mF)
 - The number of discrete capacitors is still under study at this time

Following the exercise of choosing the components to be embedded (with the knowledge that some further investigation and modeling would be completed at a later date for the capacitors), the board layout was started. Figure 5 shows the layer stack-up for this conversion.

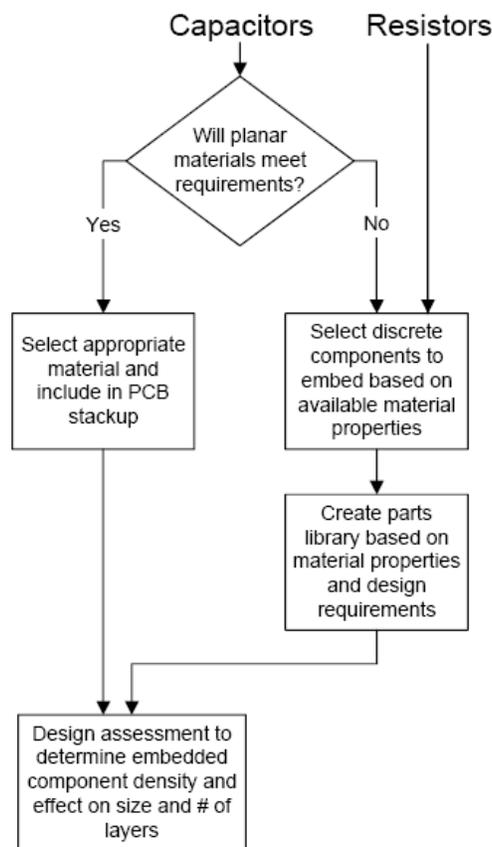


Figure 4: Decision tree describing the process on what passives to embed.

4 Embedded PCB—Layer Stack-up and Resultant Board Size

As can be seen in Figure 5, the board is fairly complicated with numerous Power and Ground Planes for both the Analog and Digital signals. Even though this portion of the board is digital by function, the total number of layers from the original design had to remain the same as it was requested that this PWB be a direct “drop-in” to the original design. Figure 5 illustrates how all individual boards are manufactured at the same time. Therefore, each small PCB (petal) would ultimately contain all of the same layers.

Layer	Description	Thickness (mils)	Material	Via Structure
	Mask	0.70		
	Plating	1.00		
1	Signal	0.35	1/4 oz ABC Foil	
	Prepreg	1.80	Arlon 1x38N8060 (106)	
2	Analog Plane (Ground)	1.40	1 oz Cu	
	Capacitor Dielectric	0.56	C-Ply (14um)	
	Resistor Metal	0.00	1000 Ohm Ticer CrSiO	
3	Analog Plane (Power)	1.40	1 oz Cu	
	Prepreg	3.00	Arlon 1x38N8060 (1080)	
	Core Dielectric	10.00	Arlon 85N 0.010" 0/0	
	Prepreg	3.00	Arlon 1x38N8060 (1080)	
4	Analog Signal	0.70	1/2 oz Cu	
	Capacitor Dielectric	0.56	C-Ply (14um)	
	Resistor Metal	0.00	25 Ohm Ticer NiCrAlSi	
5	Analog Signal	0.70	1/2 oz Cu	
	Prepreg	3.00	Arlon 1x38N8060 (1080)	
	Core Dielectric	5.00	Arlon 85N 0.005" h/h	
6	Analog Plane (Ground)	0.70	1/2 oz Cu	
	Prepreg	3.00	Arlon 1x38N8060 (1080)	
7	Digital Plane (Ground)	0.70	1/2 oz Cu	
	Core Dielectric	5.00	Arlon 85N 0.005" h/h	
	Prepreg	3.00	Arlon 1x38N8060 (1080)	
8	Digital Signal	0.70	1/2 oz Cu	
	Resistor Metal	0.00	25 Ohm Ticer NiCrAlSi	
	Capacitor Dielectric	0.56	C-Ply (14um)	
9	Digital Signal	0.70	1/2 oz Cu	
	Prepreg	3.00	Arlon 1x38N8060 (1080)	
	Core Dielectric	10.00	Arlon 85N 0.010" 0/0	
	Prepreg	3.00	Arlon 1x38N8060 (1080)	
10	Digital Plane (Power)	1.40	1 oz Cu	
	Resistor Metal	0.00	1000 Ohm Ticer CrSiO	
	Capacitor Dielectric	0.56	C-Ply (14um)	
11	Digital Plane (Ground)	1.40	1 oz Cu	
	Prepreg	1.80	Arlon 1x38N8060 (106)	
12	Signal	0.35	1/4 oz ABC Foil	
	Plating	1.00		
	Mask	0.70		
	Overall	70.74		
	Target Spec	72.00		

Figure 5: Layer stack-up for the PCB showing the materials and thicknesses as well as the via structures. The copper thicknesses were dictated by the JPL design team.

References

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