National Aeronautics and Space Administration

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JPL Publication 08-27 12/08

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NASA Electronic Parts and Packaging (NEPP) Program
Office of Safety and Mission Assurance

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NASA WBS: 939904.01.11.30
JPL Project Number: 102197
Task Number: 3.36.8

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This research was carried out at the Jet Propulsion Laboratory, California Institute of Technology, and was sponsored by the National Aeronautics and Space Administration Electronic Parts and Packaging (NEPP) Program.

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I. Introduction

In recent years there has been increased interest in the possible use of high density commercial nonvolatile flash memories in space because of their high density capabilities and data retention. They are used in a wide variety of spacecraft subsystems. At one end, flash memories are used to store small amounts of mission critical data such as boot code or configuration files. On other end of the spectrum, flash memories are used to construct multi-gigabyte data recorders that are used to record mission data.

Flash memory cells are not as sensitive to data loss, or bit upsets induced by single event effects (SEE), compared to those experienced by static random access memories (SRAMs) and dynamic random access memories (DRAMs). Information on floating gates (FGs) is embedded by the presence or absence of trapped charges on an electrically isolated conductor. Nevertheless, flash memories are susceptible to upset and degradation from radiation and more information is needed on their radiation characteristic before they can be used in space.

Because of their complex structure, flash memory cannot be treated as simple memory; therefore, it is quite challenging to determine how they respond in radiation environments. The most radiation sensitive part of flash memory is the complex circuitry external to the floating gate cell array. Different functional failures have been detected in commercial devices depending on the mode of operation during radiation exposure [1-2]. The functionality of flash memories begins to fail as total ionizing dose (TID) accumulates during a space mission. In addition, direct strikes from galactic cosmic rays (GCR) and protons from a solar flare can upset internal circuitry associated with structures such as the charge pump, state buffers, cache, or state machines. These upsets can result in incorrect read/write operation or even cause the device to not function until it is power cycled, reinitializing all the internal circuitry.

Only a limited number of high density flash memories have been subjected to radiation tests, and the majority has been older device types, which are designed with much larger feature sizes [1-5]. At present, the industry trend is to continue with feature size scaling. In advanced flash memories one would expect the single event upset (SEU) cross section to become smaller, with shrinking feature sizes and consequently improve the possibility of increase in the density. Also, because of thinner oxide layers, the total dose response is improved.

In general, one might expect the radiation response of advance high density flash memories to follow the behavior of older generations of flash including lower SEU rates and higher TID levels. However, because of the higher densities, the internal circuitry is more condensed and there is a chance of dynamic failure [2]. For highly scaled devices, the track structure of ions is comparable to the geometric size of critical regions within these highly scaled devices. One or multiple energetic ions are highly probable to hit the same critical region, transferring enough ionizing dose to create failures. In particular, this phenomenon may be on the verge of becoming a serious problem as feature size scaling becomes comparable to ion track sizes. The goal of this task is to study this phenomenon to understand the effects of scaling on dynamic failures.

II. Experimental Procedure

II.A Device Descriptions

Two basic design approaches have been used to develop high density flash memories. The first design approach uses the NOR structure. The NOR structure provides access to individual cells, which simplifies the overall device architecture but increases cell area because of the need for contacts at each drain and source connection. The NOR structure requires voltages of about 12 V for erasing and writing [6]. NOR flash memories have evolved rapidly in recent years. New design techniques such as multi-level charge storage have been proposed to increase storage density in the NOR structure and are now available commercially. The second approach uses the NAND structure. The NAND cell is more compact because it does not provide contacts to individual source and drain regions and is easier to scale to higher densities. However, cells in the NAND structure require reading and writing through the other cells in the stack, an architecture that results in inherently slower cell access. The NAND structure uses buffering and page programming to improve performance and is therefore much more susceptible to SEE. Cells in the NAND structure require higher voltages, typically about 20 V for erasing and writing [6].

High density commercial nonvolatile flash memories with the NAND and NOR architecture are now available from different manufacturers. This report examines SEE effects in high density 8 Gb single die NAND flash memory from Samsung (K9G8G08UOMPCBO) and a 512 Mb NOR flash memory from Spansion (S29GL512N10FA1010). Also, we report a new catastrophic failure mode in both NOR and NAND flash memories. The Samsung device is a multiple level cell (MLC). Table 1 summarizes the parts we studied for this report.

Table 1. Summary of NAND and NOR flash memories under study.

Device	Architecture	Feature Size (nm)	Density	Core Voltage (V)
Samsung	NAND	65	8 Gb	3.3
Spansion	NOR	130	512 Mb	3.3

II.B Test Facility

Heavy ion SEE measurements were performed at two facilities. The Radiation Effects Facility located at the Cyclotron Institute Texas A&M University (TAM) and the SEU Test Facility located at the Brookhaven National Laboratory (BNL). The TAM facility uses an 88” cyclotron while the BNL facility uses a twin Tandem Van De Graaff accelerator. Both facilities provide a variety of ion beams over a range of energies for testing. Ion beams used in our measurements are listed in Table 2 for the TAM facility and Table 3 for the BNL facility. Linear Energy Transfer (LET) and range values are for normal incident ions. At the TAM facility we used 15 MeV/amu ion beams in our tests. Beam fluence was $1x10^4$ to $1x10^7$ ions/cm^2. At the TAM facility, radiation testing was done in air with normal incident beam. The majority of high current spikes data were taken at the TAM facility. The BNL facility was used for SEU and SEFI characterization of the 8 Gb Samsung NAND flash memory and 512 Mb Spansion NOR flash memory. Tests at BNL were done at vacuum with normal incident beam.

Table 2. List of the ion beams used in our SEE measurements at the TAM facility.

Ion	LET (MeV-cm^2/mg)	Range (μm)
^{84}Kr	27.8	134
^{109}Ag	42.2	119
^{129}Xe	51.5	120
^{141}Pr	58.3	118
^{197}Au	85.4	118

Table 3. List of the ion beams used in the measurements at the BNL facility.

Ion	LET (MeV-cm2/mg)	Range (μm)
^{19}F	3.4	120
^{28}Si	8.0	74
^{48}Ti	19.8	40
^{9}Br	37.3	36
^{107}Ag	52.9	31
^{127}I	59.7	31

II.C Test Setup

The devices under test (DUTs) were etched to remove the plastic packaging and expose the memory array to the ion beam. The Samsung 8 Gb NAND data were taken using a commercial memory tester called JDI. The JDI tester is capable of performing high speed testing on memory systems. The JDI system and DUT were powered separately by an HP6629 power supply. This setup allowed for rapid detection and protection from single event latchup (SEL) events. The Spansion 512 Mb NOR data were taken using a field-programmable gate array (FPGA)-based board designed to be connected directly to the DUT. The board and DUTs were powered separately by an HP6629 power supply. Operation of the board and data transfer were carried out via an RS232 connection to a PC. This setup also allowed for rapid detection and protection from SEL events and storage of the first 1200 error addresses. The test system is described in [7].

All tests were performed by first loading the DUT with a random pattern, then verifying the pattern by reading back the device. During irradiation, the DUT was read continuously and checked for errors. All errors were logged. After the irradiation, the pattern was again verified; the device power was cycled and then erased to make it ready for the next run.

The TID delivered to the DUT by the ion beam was monitored during the heavy ion test. When the dose reached levels where the device performance was degraded, the DUT was switched to a virgin device so as not to invalidate the fidelity of the SEE test results.

III. Test Results

Three types of radiation induced events were observed while performing read operations during irradiation: SEU, single event functional interrupts (SEFI), and high current spikes, which in

some cases caused catastrophic device failure that manifested as a loss in ability to erase and write to the DUT.

III.A SEUs

SEUs were observed for all devices under test; however, the commercial high density devices appear to be much less susceptible to SEUs than typical flash devices that have been tested recently [1,3,8]. The SEU cross section per bit for these devices is on the order of $1x10^{-10}$ cm^2/bit. We also noticed that the NOR flash has less upsets than the NAND flash. These low upset rates can be easily handled by the most rudimentary error detection and correction systems. In Fig. 1, we show the SEU cross section for the Samsung 8 Gb NAND flash memory. The error bars are ~2 sigma and result from Poisson statistics. For the data points where statistical error bars are not shown, they are smaller than the size of the plotting symbols. The GCR rate is about $1.0x10^{-9}$ events per bit per year (Worst case). The rate from solar flare is about $2.0x10^{-6}$ per bit per flare (Worst case) [9].

The SEU cross section for the Spansion 512 Mb NOR flash memory is shown in Fig. 2. The error bars are ~2 sigma and result from Poisson statistics. For the data points where statistical error bars are not shown, they are smaller than the size of the plotting symbols. The NOR devices appear to be less prone to SEUs than the NAND flash under study. This is most likely attributed to the fact that the internal state machines have much simpler design in NOR devices. The GCR rate is about $2.6x10^{-10}$ events per bit per year (Worst case). The rate from solar flare is about $5.0x10^{-7}$ per bit per flare (Worst case) [9].

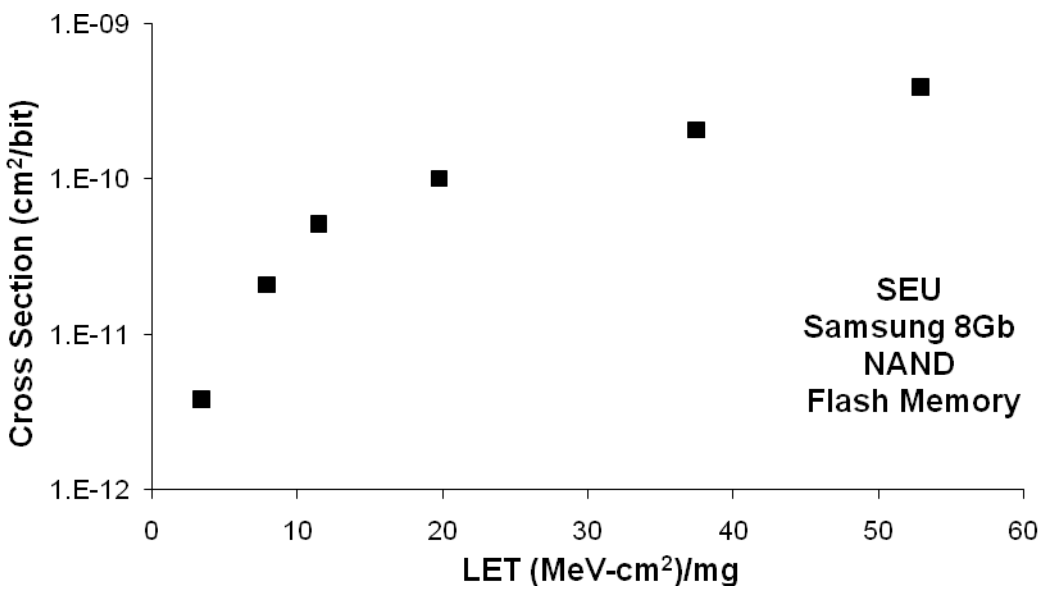

Fig. 1. SEU cross section for 8 Gb Samsung NAND flash memory. Measurements were performed at the BNL facility.

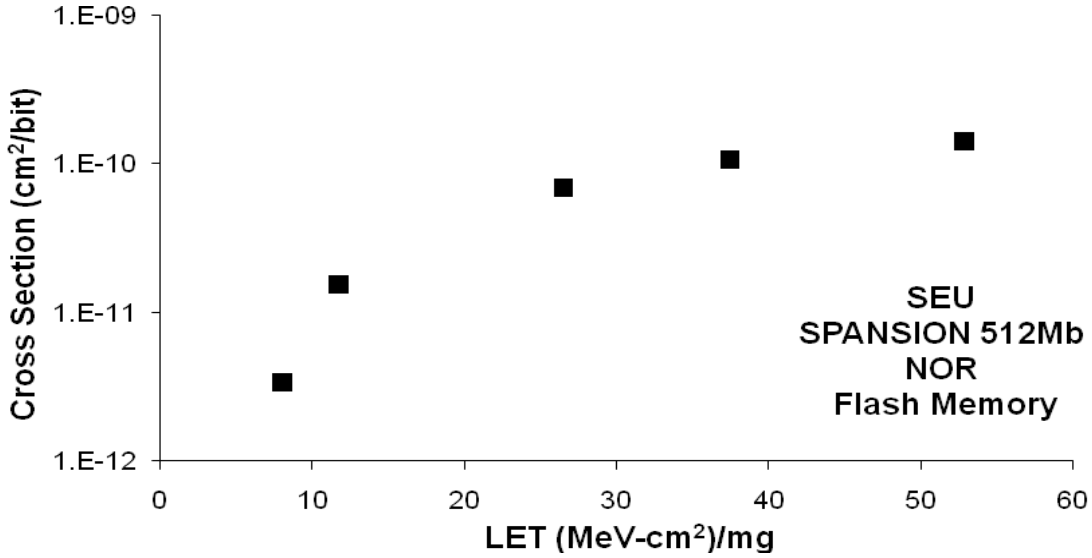

Fig. 2. SEU cross section for 512 Mb Spansion NOR flash memory. Measurements were performed at the BNL facility.

III.B SEFIs

In Fig. 3, we show the SEFI cross section for Samsung 8 Gb NAND flash memory. The error bars are ~2 sigma and result from Poisson statistics. The SEFI LET threshold is below 12 MeV-cm^2/mg. The GCR rate is about 2.0×10^{-4} events per device per year (Worst case). The rate from solar flare is about 0.35 per device per flare (Worst case) [9]. An analysis of SEFIs was complicated because it is unclear how much beam was delivered to the device before the SEFI occurred. Another analysis complication was that the signature, recovery mechanism, and consequence to the device operation varied greatly, depending upon exactly how the device functionality was altered. Typical SEFI events resulted in a large number of errors while trying to read the device. We defined the SEFI cross section as the number of times the device would experience SEFI divided by the total fluence to which the device had been exposed, including runs with no observed SEFI. This was done for each LET. Some events will self-recover once the device is re-read. Other SEFIs require a power cycle and the part to be re-initialized to return to normal operations.

The SEFI cross section for Spansion 512 Mb NOR flash memory is shown in Fig. 4. The error bars are ~2 sigma and result from Poisson statistics. The SEFI LET threshold is below 12 MeV cm^2/mg. The GCR rate is about 2.3×10^{-6} events per device per year (Worst case). The rate from solar flare is about 4.1×10^{-3} per device per flare (Worst case) [9].

The NOR devices appear to be less prone to SEFIs than the NAND flash under study. This is most likely attributed to the fact that the internal state machines have much simpler design in NOR devices.

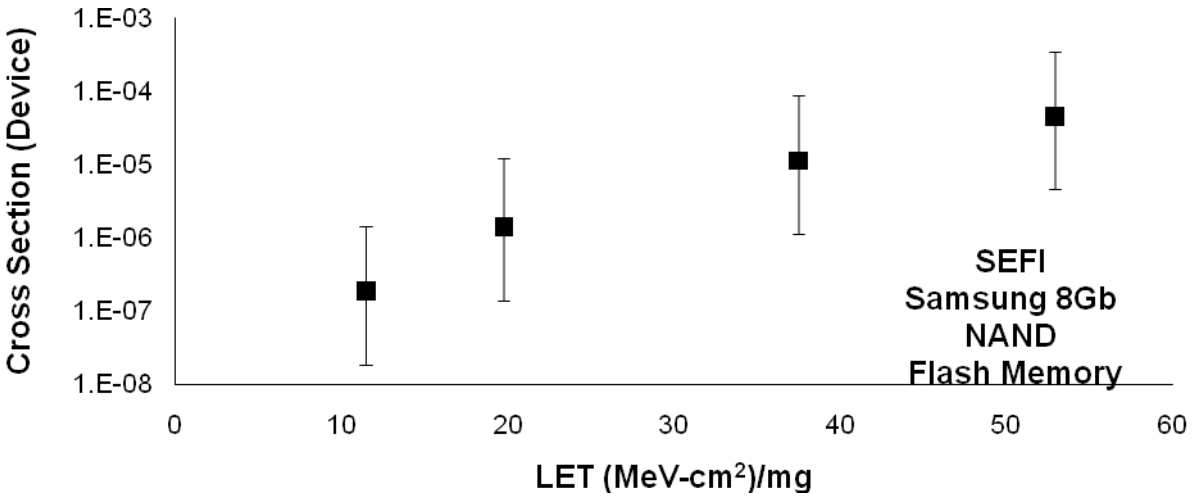

Fig. 3. SEFI cross section for 8 Gb Samsung NAND flash memory. Measurements were performed at the BNL facility.

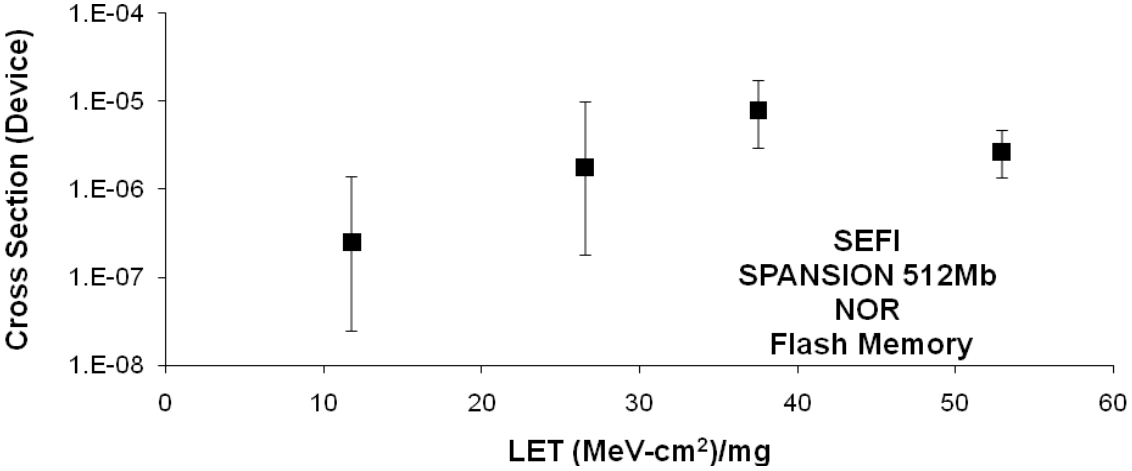

Fig. 4. SEFI cross section for 512 Mb Spansion NOR flash memory. Measurements were performed at the BNL facility.

III.C High Current Phenomenon

The most surprising and troublesome observation in our measurements was the loss of ability to erase and write to the device due to the occurrence of relatively high current spikes during high LET testing. This phenomenon even happened when the DUT was a virgin device and the dose delivered in that run was relatively low—approximately a couple of krads(Si). These flashes

were tested previously in a Co-60 chamber and survived to levels of at least 50 krad(Si) [10], thereby confirming that the phenomena is not a consequence of TID but due to single ions striking a sensitive area of the device.

This high current spikes phenomenon was observed even in static mode under bias. However, this phenomenon was not observed in static unbiased mode where flash memories were programmed before exposure. We masked the charge pump region and internal circuitry during exposure in order to investigate if the charge pump or the internal circuitry was the source of the high current spikes. No high current spikes were observed, indicating that high current spikes are caused by energetic ions hitting those regions. Fig. 5 shows typical current spectra versus time for 8 Gb Samsung NAND flash memory in static mode at LET 85 MeV-cm^2/mg, after 10^7 ^{197}Au ions per cm^2. The operating current for this device is about 0.3 mA, but during irradiation the spikes were as high as 280 mA and should not be mistaken with latchup events. Although radiation causes the current to spike, it can not stay in high current mode; our measurements show they last for less than 400 ms. This phenomenon was destructive for the Samsun 8 Gb NAND flash under study.

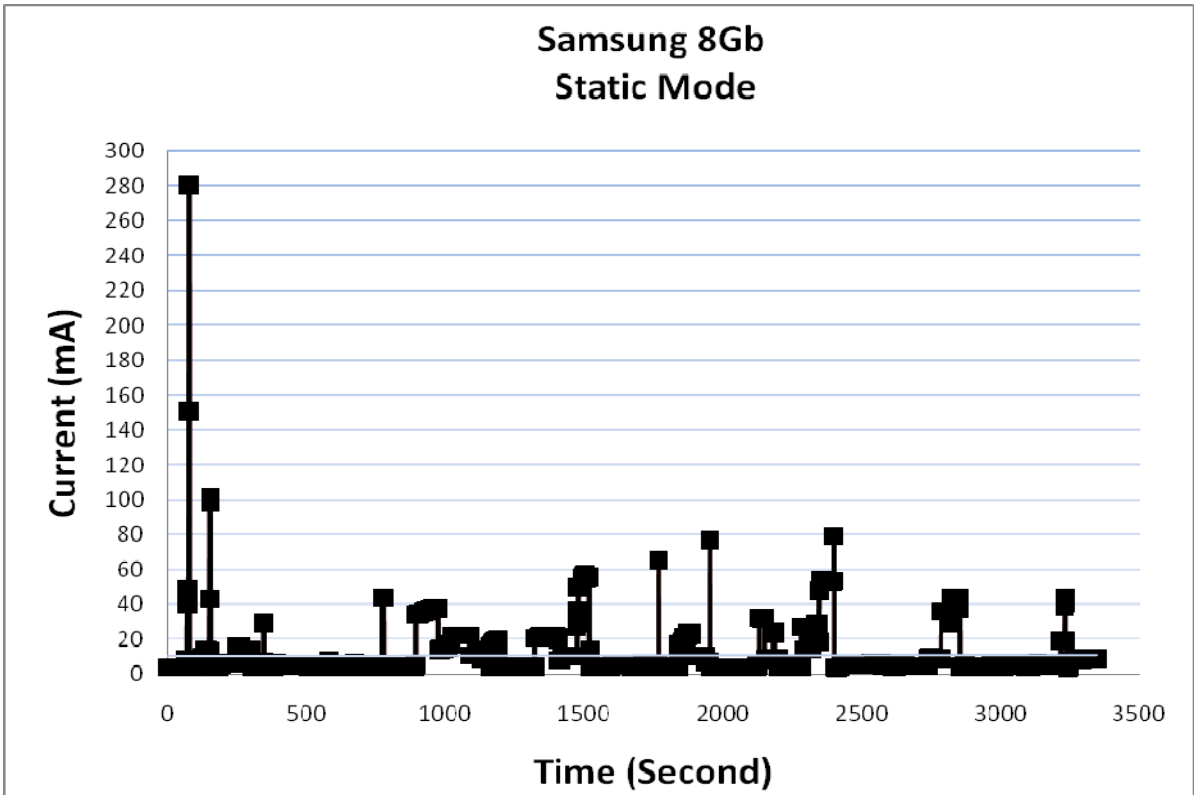

Fig. 5. Current spectrum for 8 Gb Samsung NAND flash. Data were taken with ^{197}Au ion at LET 85.4 MeV-cm^2/mg at the TAM facility.

The suspected susceptible structure is the charge pump, which is used to generate the large voltages required to erase the device. This is typically the first structure to also fail in TID testing. In this case, a single or a few particles deposit enough ionization local to the volume associated with the charge pump to produce the same degradation. In Fig. 6 we show a thermal image of a damaged device with power on. It shows damage in the charge pump region.

We also performed some limited measurements to study the directional dependence of this phenomenon. Our limited results did not follow the cosine law.

We performed measurements in two different modes: READ and PROGRAM mode. In Figs. 7 and 8 we display the cross section data for high current spikes for 8 Gb Samsung NAND flash in READ and PROGRAM mode, respectively. The LET threshold is below 27.8 MeV cm^2/mg. The cross section is higher in PROGRAM mode.

Fig. 9 shows the cross data for high current spikes for 512 Mb Spansion NOR flash in READ mode. Surprisingly, the current spike phenomenon is not destructive for this part in READ mode; however, high current spikes were destructive in PROGRAM mode for this part, but cross section data are not given.

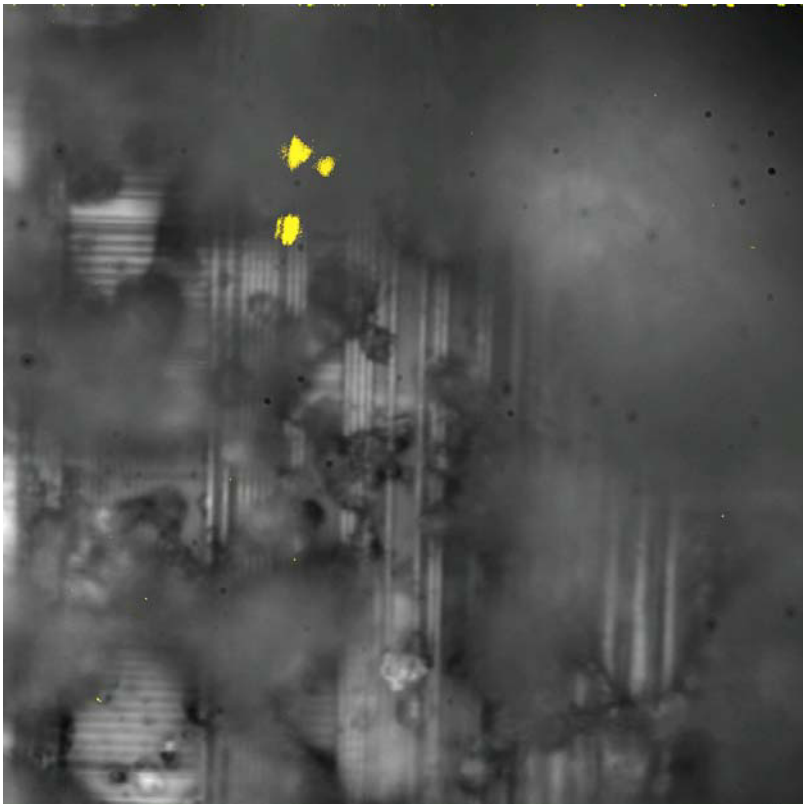

Fig. 6. Thermal picture of the charge pump region of the 8 Gb Samsung flash memory. The damaged area is clearly visible.

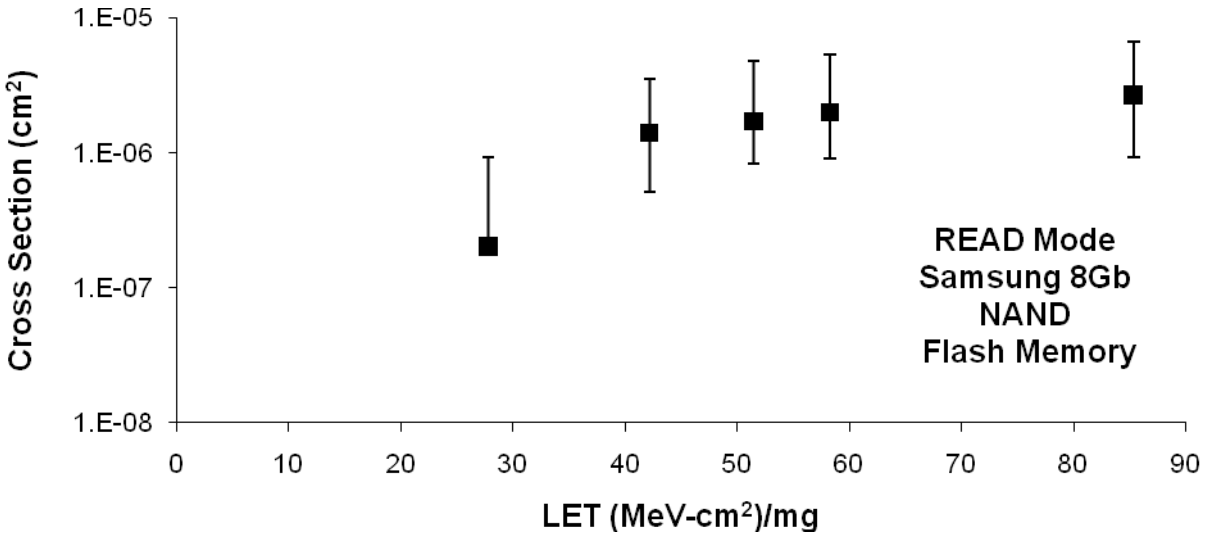

Fig. 7. Cross section for high current spikes for the 8 Gb Samsung NAND flash in READ mode. Measurements were performed at the TAM facility.

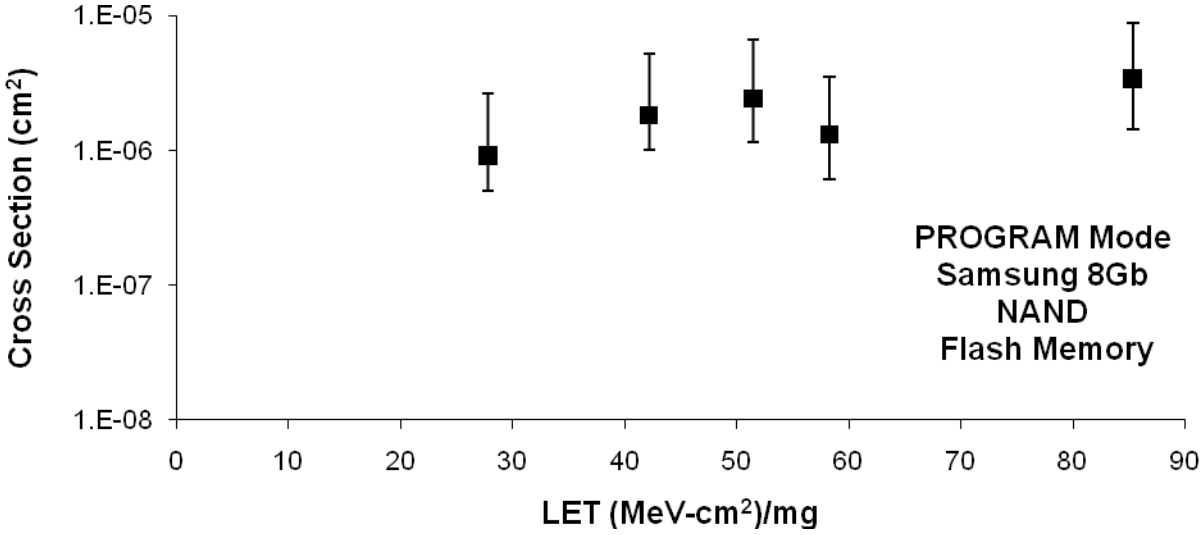

Fig. 8. Cross section for high current spikes for the 8 Gb Samsung NAND flash in PROGRAM mode. Measurements were performed at the TAM facility.

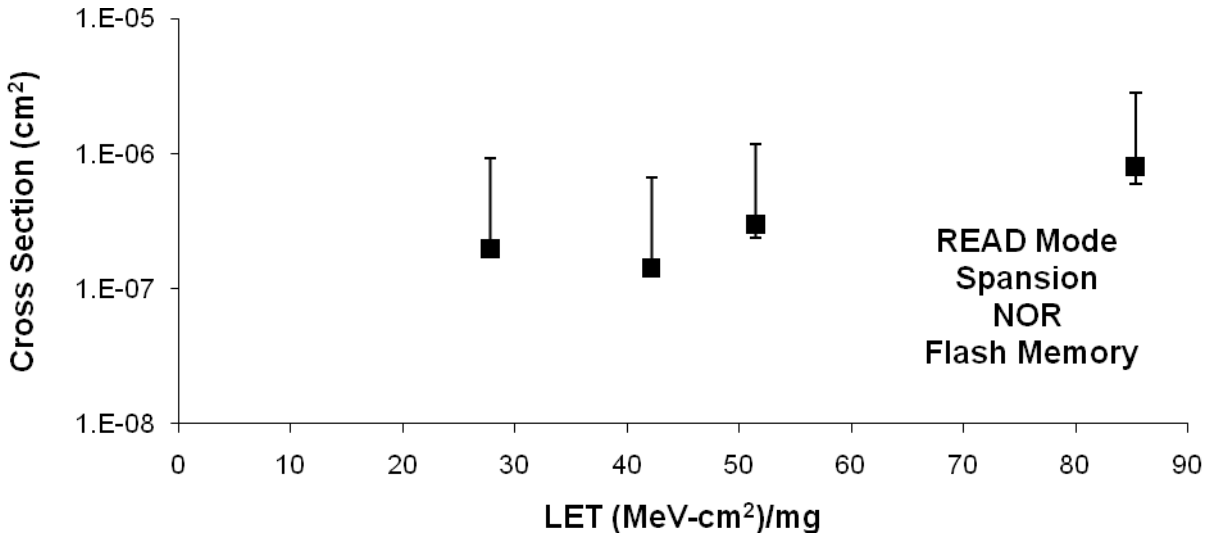

Fig. 9. Cross section for high current spikes for the 512 Mb Spansion NOR flash in READ mode. Measurements were performed at the TAM facility.

IV. TID

Total Incremental Dose (TID) tests on Samsung 8 Gb NAND flash memory were done at 25°C using the JPL Cobalt-60 facility at a rate of 25 rad(Si)/s. The DUTs were static biased during irradiation. Sequential numbers were programmed into the DUTs to simulate real world data. The TID measurements were performed in the following two modes:

1. **EPR or Refresh Mode**
   - **a**. Erase, write, and read to validate sequential numbers.
   - **b.** Irradiate with static biased DUTs.
   - **c.** Read random numbers to ensure data retention.
   - **d.** Repeat **a** to **c** for each radiation increments**.**

2. **Read Only or No Refresh Mode**
   - **a.** Erase, write, and read to validate sequential numbers.
   - **b.** Irradiate with static biased DUTs.
   - **c.** Read random numbers to ensure data retention.
   - **d.** Repeat **b** to **c** for each radiation increments.

For each mode, three devices were subjected to TID measurements. In Refresh Mode we irradiated three parts at 10 krad (Si), 20 krad (Si), 30 krad (Si), 50 krad (Si), 75 krad (Si), and 100 krad (Si). All three devices only had a few read errors. Two new devices were irradiated at different doses: 125 krad (Si), 175 krad (Si), 200 krad (Si), and 225 krad (Si). Both of the devices function, and only one had 3,035 read errors out of 8 billion bits.

In No Refresh Mode, the DUTs were subjected only to read after irradiation. Three parts were programmed with sequential numbers. Table 4 summarizes the TID results, and Fig. 10 displays the percentage of erroneous bits versus the dose.

After 12 hours annealing at room temperature, there was no recovery. All three parts were erased, programmed, and read to verify functionality. All three perform normally, and they have the following number of read errors: 13, 11, and 11, respectively.

Table 4. Summary of TID results for 8 Gb Samsung NAND flash memory for 3samples.

TID (Krad)	Errors (Sample #1)	Errors (Sample #2)	Errors (Sample #3)
10	8	9	5
20	908	8151	1868
30	498,486	269,831	757,053
40	23,602,768	85,978,925	95,856,256

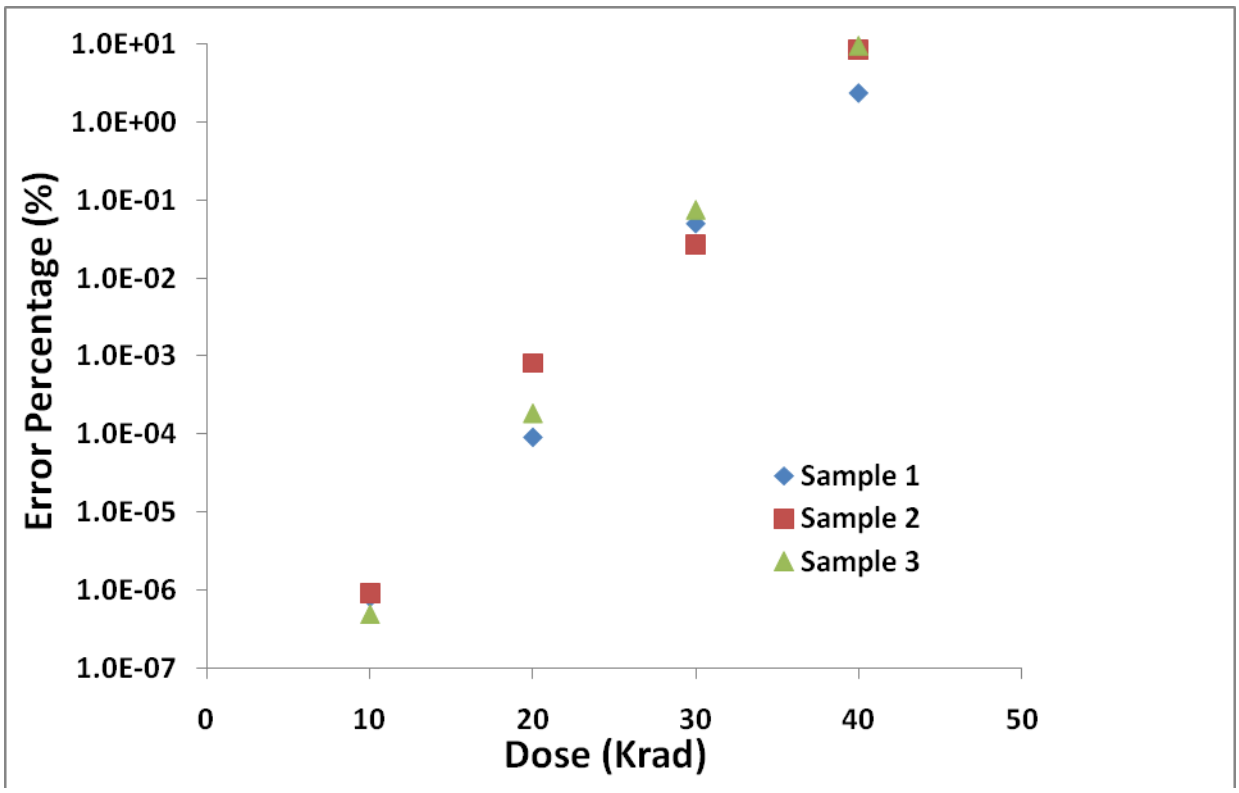

Fig. 10. Percentage of data errors versus dose for 8 Gb Samsung NAND flash.

V. Discussion

Interpretation of radiation tests in the new generation of flash memories is difficult because of the very involved architecture and internal circuitry. Heavy ion tests in earlier studies found no fundamental cell upsets; however, apparent upsets in the most complicated devices were attributed to buffer and register upsets [1,2,8]. Upset in both NOR and NAND technologies occurred in the microcontroller and register regions, causing complex errors at the block level as well as address errors. The radiation tests in the present study were more limited in scope and concentrated on determining whether the same general types of functional errors occurred in newer high density flash memories as well as investigating the possibility of destructive failures. SEU in the newer high density devices appears to be similar to that in the older technology. Functional failures caused by cell upset in the very complex control and state registers used in flash memory architecture continue to occur. It is likely that page/block SEFI type of errors arise due to upsets in configuration registers in the memory array rather than upsets of the individual bits.

The results presented above for the high current spikes and destructive behavior we observed in our study are not adequate to clearly identify the exact cause and mechanism of the phenomenon. There are several scenarios that might be able to identify the cause of the destructive high current spikes.

1- Taking into account an increasing oxide breakdown field with decreasing oxide thickness, advanced technologies should become less susceptible to single event gate rupture (SEGR) at a given electric field as gate oxide thickness decreases [11]. There is, however, a great deal of uncertainly in how the voltage may be scaled with decreasing oxide thickness. Furthermore, work by Johnston [12] raised the concern that SEGR may limit the scaling of the advanced integrated circuits (ICs). In the last few years, pioneering work has uncovered a variety of new radiation induced effects in thin gate oxides, including radiation induced leakage current in gamma and electron irradiated oxides [13], single gate rupture [12], and radiation soft breakdown (RSB) [11,14-15] in oxides exposed to high LET heavy ion irradiation. However, very few advanced ICs with thin oxides have been subjected to gate rupture experiments, and most of the conclusions about scaling are based on experiments with capacitors. Although capacitors provide insight into some aspects of the phenomena, they can not necessarily be extended directly to circuits because of the difference in geometry and doping levels [11]. The dielectric gate ruptures due to heavy ions have only recently been observed in high density digital circuits that have ultra thin oxides (less than 7 nm). Permanent damage attributed to catastrophic gate breakdown from heavy ion was first reported in [16] for 4 Mb DRAMS. Recently, the SEGR was reported in linear devices [17]. It was concluded that SEGR thresholds depend strongly on ion energy but are independent of oxide defects, bias polarity, doping concentration, and ionizing dose.

2- The micro-dose effect (localized dose deposited by one ion) can be on order of 4 to 20 Krads [18-20]. The micro-dose effect is more probable for scaled devices. For scaled devices such as the flash memories under study in this work, the track structure of ions is comparable to the geometric size of critical regions within these highly scaled devices. One or multiple energetic ions are highly probable to hit the same gate, transferring enough ionizing dose to create failures. However, much of the data is suggestive of

damage in the charge pump region or control circuitry for the devices tested here. This is typically the first structure to also fail in TID testing.

3- This phenomenon might be attributed to the doping level in the Samsung 8Gb flash memory. It has been shown the critical voltage condition for breakdown is somewhat lower for higher doping concentrations than for low doping [12]. The Samsung 8Gb flash memory might have higher doping level and consequently lower critical voltage condition.

The observed phenomenon in advanced flash memories might be indicative of standard flash memory response coming in future generations. This is likely a result of the scaling down of feature size, oxide thickness, and the number of electrons trapped on the floating gate [21]. As flash cell sizes are decreased, the nature of this phenomenon and its effects might become significant.

VI. Conclusion

We tested the advanced commercial high density 8 Gb NAND flash memory from Samsung with heavy ions. We also tested the advanced commercial NOR flash memory from Spansion. The general conclusion is that the SEU and SEFI cross section is smaller than the older generation of flash memories.

Another observation is a new high current phenomenon in the high density NAND and NOR flash memories. This high current phenomenon is destructive for Samsung NAND flash memory during READ and PROGRAM modes and during PROGRAM mode for Spansion NOR flash.

The results in this report show that the high current phenomenon in scaled devices is a complex problem that is not fully understood. Processing details and oxide defects appear to play a role in gate rupture, and the differences in experimental observations by different groups may be because of difference in semiconductor processing. More work needs to be done to increase the level of understanding as well as how it may affect highly scaled commercial devices. The high current spikes phenomenon is on the verge of becoming a serious problem as scaling continues and the transistors sizes become comparable to ion track widths.

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